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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

	JOSEPH T. EVANS, JR. ET AL.
Serial No.:	582,672
Filed:	September 14, 1990
Group/Class:	233
Examiner:	Alyssa H. Bowler
For:	NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure, Applicants wish to bring to the attention of the Examiner the following patents which may be material to the above-identified application. The patents are listed on the attached PTO Form 1449. Copies of the listed patents are enclosed herewith.

U. S. Patent 4,860,254 by Pott et al. Disclosed in this patent is a technique for integrating into a monolithic circuit volatile and non-volatile memory elements. A standard single-transistor DRAM cell, which defines a volatile memory element, is integrated with a

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Signature

Aug 12 1991
Date of Signature

ferroelectric capacitor, which defines the non-volatile storage element. Information can be transferred from the volatile DRAM section to the ferroelectric capacitor, and vice versa.

U. S. Patent 4,477,886 by Au. This patent discloses what is apparently a dynamic random access cell, in which the capacitors of the cells are recharged by lines other than the standard bit line.

U. S. Patent 4,408,303 by Guterman et al. A capacitively coupled non-volatile static ram cell includes standard cross-coupled transistors to store volatile data. A series-connected standard capacitor and tunneling capacitor arrangement is connected to each of the switching transistors to store data in a non-volatile manner. During regular volatile operation, the supply voltage is maintained at about five volts, while during the non-volatile store operation, the supply voltage is ramped up to about 20 volts, thereby forcing each tunnel capacitor into different states. The memory cell has a write, read, store and recall mode of operation.

U. S. Patent 3,832,700 by Wu et al. The ferroelectric memory device disclosed in this patent replaces the standard MOS transistor gate insulator with a ferroelectric dielectric material which exhibits hysteresis characteristics. When the ferroelectric material is polarized in one direction, the transistor functions as a normally closed switch, and when polarized in the opposite direction, the transistor remains off.

U. S. Patent 4,161,038 by Wu. This patent discloses a CMOS transistor structure where both transistors are fabricated with gate insulators of ferroelectric material.

The transfer function of each transistor can be varied by appropriate polarization of the ferroelectric gate insulators. The device is thus programmable to remember or store the value of a reference signal for subsequent comparison with an input signal which is applied as a threshold voltage to the complementary CMOS device.

U. S. Patent 2,938,194 by Anderson. This patent discloses a technique for accessing ferroelectric capacitors in a two-dimensional storage matrix. A particular capacitor is selected for the storage of information by applying a voltage of one polarity to one of the row leads of the matrix, and applying a voltage of the opposite polarity to a column lead. The two voltages are individually insufficient to reverse the polarization of the ferroelectric capacitors, but when occurring together are sufficient to reverse the polarization thereof. A third voltage can be applied across the capacitor of sufficient voltage and proper polarity to cause a return to the initial state of polarization of the ferroelectric material, thus reading out the information stored in the capacitor.

U. S. Patent 4,873,664 by Eaton, Jr. The Eaton patent discloses a ferroelectric memory structure having columns of ferroelectric memory cells with complementary bit lines connected to respective sense amplifiers. Each ferroelectric memory cell includes a pair of series-connected switching transistors and associated ferroelectric capacitors connected to a respective complementary bit line. Complementary binary data is stored in each cell during a write operation, and is destructively read during a read operation. By the

application of appropriate signals to the capacitor plate lines, the sense amplifier is effective to restore the data states in the accessed cell subsequent to a read operation.

British Patent Specification 1,544,314 by Uchida et al. This British patent specification discloses a non-volatile semiconductor memory device which includes a bistable latch and a pair of binary capacitors. The capacitors are written with polarization states by applying a -25 volt level to the MG control signal line, in which event the hysteresis thresholds of the capacitors develop different voltages, depending upon the binary state of a corresponding pair of nodes. During power up, the signal stored in the capacitors can be returned to preset the nodes to predefined digital states.

Publications

Hybrid Volatile/NonVolatile Integrated Memory Arrays, IBM Technical Disclosure Bulletin, Vol. 18, No. 5, October, 1975. This technical article discloses a cell arrangement having volatile and non-volatile sections. The volatile section is defined by a set-reset flip-flop, the complementary outputs of which are connected across a ferroelectric capacitor in series with a switching transistor element. During normal operation, the ferroelectric capacitor stores the state of the flip-flop output, and stores the last state thereof before power down. The state of the ferroelectric capacitor can be transferred back to the flip-flop when powered up.

Applicants respectfully submit that the invention described in the above-identified application is distinguishable over the prior art know to Applicants and that disclosed in this statement.

Attached hereto are copies of PTO 1449 forms and associated Information Disclosure Statement previously filed in related cases.

Respectfully submitted,

RICHARDS, MEDLOCK & ANDREWS

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